What is claimed is

1. A buffering apparatus comprising:

an asynchronous data bus write unit which, when control information indicating a request for writing in a buffer connected to an asynchronous data bus not synchronized with a processor is provided by a multiplexer connected to the processor, receives third data from the multiplexer, stores the third data, and transfers the stored third data to a second memory through the asynchronous data bus; and

an asynchronous data bus read unit which, when control information indicating a request for reading from the buffer is provided by the multiplexer, receives fourth data from the second memory through the asynchronous data bus, stores the fourth data, and transfers the stored fourth data to the multiplexer.

2. A processor bus connection method comprising:

(a) when address information indicating an address of a first memory connected to a synchronous data bus synchronized with the processor, from the processor is received, receiving first data from the processor and transferring the received first data to the first memory through the synchronous data bus, or receiving second data from the first memory through

the synchronous data bus and transferring the received second data to the processor; and

(b) when address information indicating an address of a second memory connected to an asynchronous data bus not synchronized with the processor, from the processor is received, receiving third data from the processor, transferring the third data, storing the transferred third data, and transferring the stored third data to the second memory through the asynchronous data bus, or receiving fourth data from the second memory through the asynchronous data bus, storing the fourth data, transferring the stored fourth data, receiving the transferred fourth data, and transferring the received fourth data to the processor.

3. The processor bus connection method of claim 2, wherein (a) comprises:

(a1) when the address information indicating the address of the first memory is provided by the processor and the control information indicating the request for writing in the first memory is provided by the processor, receiving the first data from the processor and transferring the received first data to the first memory through the synchronous data bus; and

(a2) when the address information indicating the address of the first memory is provided by the processor and the control information indicating the request for reading from the first memory is provided by the processor,

receiving the second data from the first memory through the synchronous data bus and transferring the received data to the processor.

4. A synchronous bus and asynchronous bus path method comprising:

(a) receiving input data and transferring the received input data through a synchronous bus synchronized with a processor;

(b) receiving the input data through the synchronous bus and transferring the received input data;

(c) generating first data or third data from the transferred input data and transferring the generated first or third data;

(d) receiving the first data, transferring the received first data to a first memory through the synchronous data bus, or receiving and storing the third data and transferring the stored third data to a second memory through an asynchronous bus not synchronized with the processor;

(e) receiving the first data through the synchronous bus and storing the data; and

(f) receiving the third data through the asynchronous bus and storing the data.

5. The method of claim 4, further comprising:

(g) transferring second data through the synchronous bus;

(h) transferring fourth data through the asynchronous bus;

(i) receiving the second data through the synchronous bus and transferring the received second data, or receiving the fourth data through the asynchronous bus, storing the fourth data, and transferring the stored fourth data;

(j) generating output data from the second data or fourth data and transferring the output data;

(k) receiving and storing the output data and transferring the stored output data through the asynchronous bus; and

(l) receiving the output data through the asynchronous bus and outputting the received output data, or receiving the third data from the second memory through the asynchronous bus and outputting the received third data.

6. The method of claim 5, wherein if the received output data or the received third data is display data, the received output data is displayed.

7. The method of claim 5, further comprising:

(m) giving permission on the use of the synchronous bus; and

(n) giving permission on the use of the asynchronous bus.

8. The method of claim 7, wherein in (a), the received input data is transferred through the synchronous bus for which permission to use is given in (m); in (b), the input data is received through the synchronous bus for which permission to use is given in (m); in (d), the received first data is transferred to the first memory through the synchronous data bus for which

permission to use is given in (m), or the stored third data is transferred to a second memory through the asynchronous bus for which permission to use is given in (n); in (d), the first data is received through the synchronous bus for which permission to use is given in (m) and stored; and in (f), the third data is received through the asynchronous bus for which permission to use is given in (n) and stored.

9. The method of claim 8, wherein in (g), the second data is transferred through the synchronous bus for which permission to use is given in (m); in (h), the fourth data is transferred through the asynchronous bus for which permission to use is given in (n); in (i), the second data is received through the synchronous bus for which permission to use is given in (m) and the received second data is transferred, or the fourth data is received through the asynchronous bus for which permission to use is given in (n), stored, and the stored fourth data is transferred; in (k) the output data is received and stored, and the stored output data is transferred through the asynchronous bus for which permission to use is given in (n); and in (l), the output data is received through the asynchronous bus for which permission to use is given in (n) and the received output data is output to a user, or the third data from the second memory is received through the asynchronous bus for which permission to use is given in (n) and the received third data is output.

10. A computer readable recording medium including a computer program having instructions for controlling a synchronous bus and asynchronous bus, the instructions comprising:

(a) receiving input data and transferring the received input data through the synchronous bus synchronized with a processor;

(b) receiving the input data through the synchronous bus and transferring the received input data;

(c) generating first data or third data from the transferred input data and transferring the generated data;

(d) receiving the first data, transferring the received first data to a first memory through the synchronous data bus, or receiving and storing third data and transferring the stored third data to a second memory through an asynchronous bus not synchronized with the processor;

(e) receiving the first data through the synchronous bus and storing the data; and

(f) receiving the third data through the asynchronous bus and storing the data.